TRENCH CORNER EFFECT BIDIRECTIONAL FLASH MEMORY CELL

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to memory cells and in particular the present invention relates to structures of non-volatile memory cells.

BACKGROUND OF THE INVENTION

[0002] In order for memory manufacturers to remain competitive, memory designers must constantly increase the density of flash memory devices. Increasing the density of a flash memory device generally requires reducing spacing between memory cells. It is becoming increasingly difficult to further reduce spacing between memory cells. Closer packing also generally requires smaller dimensions of device elements.

[0003] Smaller dimensions of many device elements may cause operational problems with the cell. For example, the channel between the source/drain regions becomes shorter possibly causing severe short channel effects. Additionally, smaller size cells with a continuous layer of oxide-nitride-oxide (ONO) may have a problem with charge migrating from one bit-storage point to the other.

[0004] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for smaller non-volatile memory cells without the disadvantages inherent in the smaller cells.

SUMMARY

[0005] The above-mentioned problems with increasing memory density and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0006] The present invention encompasses a trench corner effect, bidirectional flash memory cell. The cell comprises a trench formed in a silicon substrate. A trapping material is deposited on the corners of at least two sides of the trench. The trench is filled with an

oxide material. A plurality of active areas are located on the silicon substrate. The active areas are substantially adjacent to an opening of the trench and substantially adjacent to the trench sides having the trapping material. A control gate is located above the trench. In one embodiment, the control gate partially overlaps each of the active areas.

[0007] Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 shows a cut-away view of one embodiment for a trench corner effect bidirectional flash memory cell of the present invention.

[0009] Figure 2 shows a top view of the trench corner effect bidirectional flash memory cell of Figure 1.

[0010] Figure 3 shows one embodiment of the theory of operation of the trench corner effect bidirectional flash memory cell of Figure 1 during a programming operation.

[0011] Figures 4A and B show plots of silicon-oxide interface potential versus distance along the cell having no bias and a gate bias only.

[0012] Figures 5A and B show plots of silicon-oxide potential versus distance along the cell with a drain/source bias applied simultaneously with a gate bias.

[0013] Figures 6A and B show plots of silicon-oxide interface potential versus distance along the cell with a drain/source bias applied simultaneously with a gate bias and trapping has occurred.

[0014] Figure 7 shows a plot of silicon-oxide interface potential versus distance along the cell with a drain and source bias applied to reduce both the drain-side and source-side energy barriers.

[0015] Figure 8 shows an alternate embodiment trapping layer configuration of the embodiment of Figure 1.

[0016] Figure 9 shows an alternate embodiment gate configuration for the trench corner effect bidirectional flash memory cell of the present invention.

[0017] Figure 10 shows another alternate embodiment gate configuration for the trench corner effect bidirectional flash memory cell of the present invention.

[0018] Figure 11 shows yet another alternate embodiment gate configuration for the trench corner effect bidirectional flash memory cell of the present invention.

DETAILED DESCRIPTION

[0019] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer or substrate, used in the following description, include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms wafer or substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0020] Figure 1 illustrates a cut-away view of the structure of the of the trench corner effect, bidirectional flash memory cell of the present invention. The cell can be created as

either a p-channel device or an n-channel device. The n-channel device provides for hole trapping while the p-channel device involves electron trapping.

[0021] The cell is comprised of a trench 101 that is oxide 102 filled. In alternate embodiments, the trench is filled with other low-trap-density dielectric materials.

[0022] On either side of the trench 101 are drain/source regions 103 and 104. These are either n+ or p+ regions, depending on the type of device as discussed previously. In one embodiment, the trench extends to a depth at least that of the drain/source regions 103 and 104. Since the memory cell of the present invention is a symmetrical device, the drain/source regions 103 and 104 are interchangeable. The applied voltage determines which side is the drain and which is the source. Therefore, the subsequent discussion of these areas does not limit the present invention to any one configuration of drain and source regions.

[0023] Trapping layers 109 and 110 are formed on either side of the trench 101. These layers 109 and 110 are electrically isolated sections so that there is no migration of charges from one trapping layer 109 or 110 to the other 110 or 109. As will be discussed subsequently, a data bit can be stored in each corner of the trench in its respective trapping layer 109 or 110.

[0024] In one embodiment, the trapping layers 109 and 110 are formed as substantially uniform layers covering entire opposing sidewalls of the trench. There is no trapping material across the bottom of the trench 101. In an alternate embodiment, there is at most minimal trapping material across the bottom of the trench so that the two trapping layers 109 and 110 remain isolated from each other. In another alternate embodiment, the trapping layers 109 and 110 may be formed as a continuous layer of trapping material.

[0025] Figure 8 illustrates another embodiment of the trapping layers. In this embodiment, the trapping layers 801 and 803 are formed only in the trench corners since this is where the charge build-up occurs.

[0026] Referring again to Figure 1, the type of trapping material 109 and 110 depends on the type of cell. For example, a p-channel device might use an Oxide-Nitride-Oxide (ONO)

structure. An n-channel device might use a different trapping structure. The present invention is not limited to any one type of trapping structure.

[0027] A control gate 107 of the cell of Figure 1 is formed over the oxide-filled trench 101 and overlaps the drain/source regions 103 and 104. Alternate embodiments for forming the gate structure are discussed subsequently.

[0028] Figure 2 illustrates a top view of the trench corner effect, bidirectional flash memory cell of Figure 1. This view shows the gate structure 107 overlapping the two drain/source regions 103 and 104.

[0029] Figure 3 illustrates one embodiment of the theory of operation, during a programming operation, of the trench corner effect bidirectional flash memory cell of Figure 1. In this embodiment, the substrate (V_b) is biased at less than 0V, the gate voltage V_g is 0V (or less than 0V) and the source voltage V_s is also 0V. The drain voltage V_d is biased at a typical programming voltage. In one embodiment, this voltage is in a range of 6.0 – 8.5V. These voltages are for purposes of illustration only. The present invention is not limited to any one set of voltages.

[0030] When a sufficiently high voltage is applied to the drain region, junction 301 breakdown occurs. The resulting charges are accelerated 303 towards the substrate due to the drain-to-substrate voltage. Some of the charges that are accelerated towards the substrate are redirected and trapped in the oxide near the silicon-oxide interface along the side of the trench. In one embodiment, the trapping occurs at or near the trench corner 305 in the trapping layer. This trapped charge, being opposite in polarity to the channel-type, lowers the drain-side energy barrier. The drain voltage further eliminates the drain-side energy barrier. Even though this is typically not a desirable effect for an isolation trench, it is utilized in the memory cell of the present invention as described subsequently with reference to Figures 4 – 7.

[0031] Figures 4 – 7 illustrate plots of silicon-oxide interface potential versus distance across the cell. The silicon-oxide interface potential along the y-axis, increasing from bottom to top. The distance across the x-axis of the cell is typically measured in microns and increases from left to right. The plot's corresponding cell with its trench and active

areas is not shown for purposes of clarity but the elements of the cell are indicated by the voltage indicators (i.e., V_s, V_g, and V_d).

[0032] Figure 4A illustrates a plot of silicon-oxide interface potential versus distance for a cell without a gate voltage applied. Both V_s and V_d are 0V as well. The corner affect is not yet evident since there is no gate voltage to perturb the interface potential.

[0033] Figure 4B illustrates the same plot as V_g is increased. The dotted lines indicating the change in the silicon-oxide interface potential as V_g increases. The top dotted line is where $V_g = 0$. As V_g increases from 0, it begins to perturb the potential. In one embodiment, when $V_g = 14V$, the two corner energy barriers 401 and 402 are fully evident and current flow is unaffected by the center region of the cell. This embodiment shows that V_s and V_d are both 0V and the corner energy barriers 401 and 402 are not affected.

[0034] Figures 5A and B illustrate forward and reverse bias plots of silicon-oxide interface potential versus distance for a cell with an initial drain/source bias simultaneously with a gate bias. Figure 5A shows the forward bias plot of the drain bias applied simultaneously with the gate bias. As the drain bias is increased, the drain energy barrier is pulled down further. Figure 5B shows the reverse bias plot of the source bias applied simultaneously with the gate bias. As the source bias is increased, the source energy barrier is pulled down further.

[0035] In both forward and reverse bias cases, illustrated in Figure 5, the barrier closest to the drain/source is pulled down but the opposite barrier remains high since charges have not been trapped. This prevents current from flowing along the channel and neither bit can be read.

[0036] Figures 6A and B illustrate forward and reverse bias plots of silicon-oxide interface potential versus distance along the cell with a drain/source bias applied simultaneously with a gate bias and trapping has occurred. Figure 6A illustrates the forward biased condition with a sufficient drain voltage applied, simultaneously with a gate voltage, to eliminate the drain-side energy barrier. In this case, no current flows due to the source-side energy barrier remaining high and blocking current.

[0037] Figure 6B illustrates the reverse biased condition with the source-side energy barrier pulled down by a sufficient source voltage. In this case, the drain-side energy barrier is eliminated by the trapped charge. Therefore, drain-side stress results in reverse current only.

[0038] Figure 7 illustrates a plot of silicon-oxide interface potential versus distance along the cell when a charge is trapped in both corners. The device will conduct in either direction, depending on which end is biased.

[0039] In the above embodiments of Figures 4 – 7, a sufficient drain/source voltage to pull down the respective energy barrier to allow current to flow may be in the range of 6.0V to 8.5V. Alternate embodiments use other voltage ranges to obtain substantially similar results, depending on the type of memory device. It should be noted that the reverse current may saturate at a predetermined source voltage in each of the above cases.

[0040] The trench corner effect bidirectional flash memory cell could be programmed and erased using methods substantially similar to parasitic field devices. Programming (charge trapping) could be accomplished by junction breakdown as described above. The effect can be accelerated by applying a substrate voltage or a negative V_g bias for an n-channel device.

[0041] Reading the memory cell could be performed by applying a gate voltage sufficient to invert the trench bottom center as shown in Figures 6 – 7. A voltage is also applied to the drain that pulls down the drain-side barrier. Current would then flow depending on whether there is a trapped charge present at the source-side barrier.

[0042] Erasing the memory cell could be accomplished in multiple ways. One erase method would be to tunnel the charge out of the trapping layer into the substrate by applying a voltage between the gate and the substrate/drain/source so as to produce a high electric field in the trapping material.

[0043] A second erasing method includes using hot-carrier effects by pulling significant channel current such that a charge of the opposite polarity as the trapped charge would be injected into the trapping material and compensate/combine with the trapped charge.

[0044] Figure 9 illustrates an alternate embodiment gate configuration for the trench corner effect bidirectional flash memory cell of the present invention. In this embodiment, the gate 901 is formed such that it extends down into the trench in a "T" configuration.

[0045] Figure 10 illustrates another alternate embodiment gate configuration for the trench corner effect bidirectional flash memory cell of the present invention. In this embodiment, the gate 1001 is formed within the oxide dielectric material 1003.

[0046] Figure 11 illustrates yet another alternate embodiment gate configuration for the trench corner effect bidirectional flash memory cell of the present invention. In this embodiment, the gate 1101 and 1102 is formed in two parts. One part 1102 formed within the oxide dielectric material 1110 in the trench. The other part 1101 is formed over the trench and overlapping the two active areas 1104 and 1105.

[0047] In the embodiments of Figures 9 – 11 above, an oxide material is illustrated between the trapping material along the sidewalls of the trench and the portion of the control gate extending into the trench. This oxide is not required for proper operation of the present invention. The gate may be in contact with the trapping material.

CONCLUSION

[0048] In summary, the non-volatile memory cell architecture of the present invention uses a trench corner barrier effect to produce a compact cell containing two logical bits. The absence or presence of the energy barrier, in response to the absence or presence of trapped charges, creates the non-volatile memory states.

[0049] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.